VIRGINIA STATE UNIVERSITY
COMPUTER ENGINEERING
### CPEG 207 DIGITAL SYSTEMS FALL 2020 TEST #1

Name:_____

To get full credit , you must show your detailed work and identify your answers.

1. A) Determine whether the following statements are **True (T)** or **False (F)**:

Answer:

- (a) The output of an XNOR gate is LOW when its inputs are LOW.
- (b) The output of a 3-input NAND gate is LOW when all its input are LOW.
- (c) If the inputs of a NOR gate are tied together, then the output waveform will be the complement of the input signal.
- (d) The largest decimal number that can be represented using 12 bits is 4096.
- (e) The minimum number of bits that are needed to represent the decimal number 1023 is 10.

1. B) Draw the output waveforms for each logic gate shown below:
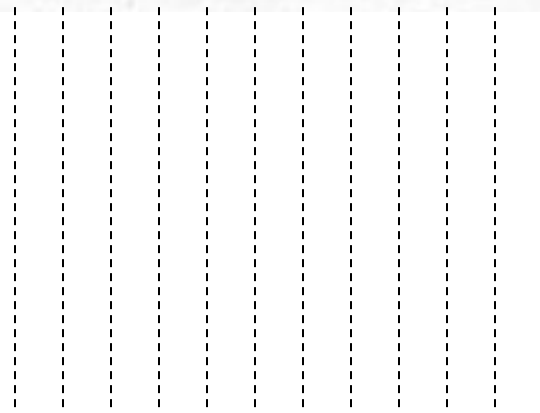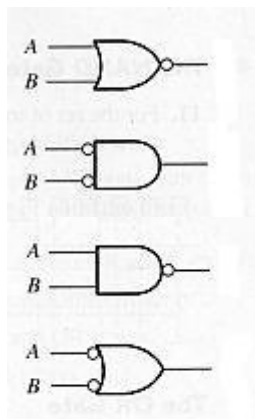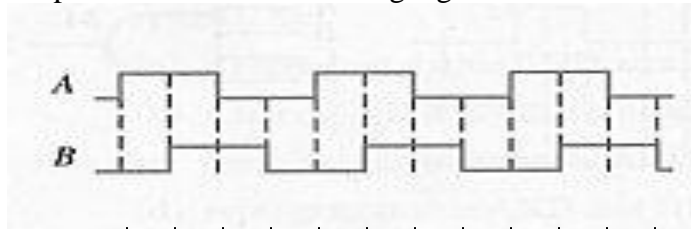
2.   a)   Convert the following binary number to decimal:
     1111111.111

                              Answer:

     Convert the following decimal number to a binary number:
     111

                              Answer:

     b)   i) Convert the decimal number 85.125 to a single precision floating point number.
          Answer:

ii) Express the following single precision floating point number as a decimal number:

1	10000001	01101000000000000000000

Answer: (Decimal)

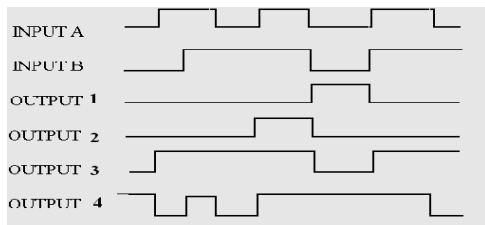c) Complete each row of equivalent numbers in the following table:

Decimal	Binary	Hexadecimal	BCD
10			
		2F	
	1111		

d) i) Perform the following Hexadecimal subtraction and give the answer in hex.

$FD_{16} - 88_{16} =$

ii) Add the BCD numbers $01100111 + 01010011$ Answer =

3.a) For a two-input XNOR gate, with the input waveforms as shown below, which output waveform is correct?   1   2   3   4

3.b) Name the gates and draw the output waveforms for the digital circuits shown below:
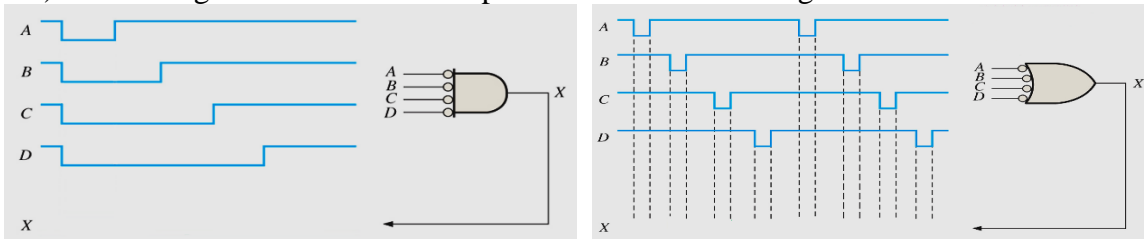
3.c) Complete the following VHDL program:

$$X = A\bar{B} + \bar{A}B$$
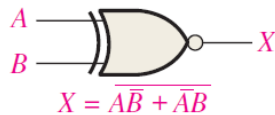
```
entity          is
    port (      : in bit;   : out bit);
end entity         ;
architecture            of        is
begin
    X <=
end architecture           ;
```

3. d) By analyzing the timing diagrams, determine whether or not the gates are faulty and **draw an arrow indicating the faulty bit time period.**

(a)

(b)

(c)

(d)

4. Design a logic circuit for a seatbelt warning indicator in a car with the following specifications: If the driver is present and the driver is not buckled up and the ignition switch is on, then turn on the warning light.

Write the Boolean expression for your seatbelt warning system.

Draw the Truth Table;

Complete the timing diagram:

Timing diagram

Name	Val	1.0 ms	2.0 ms	3.0 ms	4.0 ms	5.0 ms	6.0 ms	7.0 ms	8.0 ms	9.0 ms	10 ms
ignition_on	0										
buckled_up	0										
driver_present	1										
warning_light	0										