Laboratory No. 2 Combinational SSI Circuits

Introduction

In this set of experiments you will design and build simple circuits on Emona netCIRCUITlabs board. In experiment 1, given a logic function as a minterm list you are asked to find the corresponding minimal sum-of-products expression. You will analyze the circuit by drawing the waveforms and eliminate the static-1 timing hazard preset present. In experiment 2, the circuit with the timing hazard eliminated will be implemented in hardware. In experiment 3, a second circuit will be also analyzed starting from its hardware implementation. In the final report, please organize your content in a good format along with sufficient explanation.

The theoretical background required for this lab

- Boolean algebra
- Karnaugh maps
- Minimizing sum-of-products
- Minimizing product-of-sums
- Static timing hazards

is available from your lecture notes and textbook.

Experiments

Experiment 1: (*40 Points*)

You are given the following logic function as a minterm list

$$F(A,B,C,D) = \sum_{A,B,C,D}(1,3,5,6,7,14) \quad (1)$$

i. Starting from the minterm list, complete the truth table and derive the Karnaugh map of the function. Find the minimal sum-of-products expression for $F(A,B,C,D)$. Show your work with a nice Karnaugh map and necessary description in your lab report.

A	B	C	D	$F(A,B,C,D)$
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	

0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

ii. The circuit implementing of the above expression has been shown in Fig. 1. Analyze the static-1 timing hazard at the 0111 to 0110 transition, where the clock cycle is taken to be 100us. Assume that all the gates have the same 10ns propagation delay for any transition. Draw the following waveforms (in this order): A, B, C, D, AP, DP, DAP, BCDP, and F. Specify the time scale! (hint: should be similar to the waveforms in the textbook)

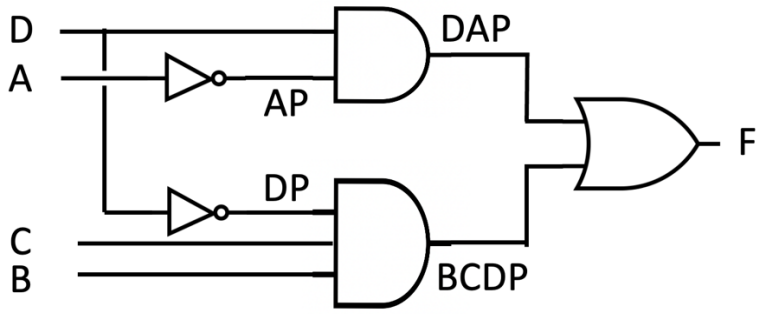

Fig. 1, circuit implementing of Eq. (1)

iii. There is a static-1 timing hazard at the 0111 to 0110 transition, so you should be careful when analyzing this step. Explain why it happened. Using the Karnaugh map, define the expression of $G(A, B, C, D)$ in which the timing hazard is eliminated. Show your work with a nice Karnaugh map and necessary description in your lab report.

iv. The circuit implementing of $G(A, B, C, D)$ has been shown in Fig. 2. Analyze the 0111 to 0110 transition again. Draw the following waveforms (in this order): A, B, C, D, AP, DP, DAP, BCDP, BCAP, and G. Has the updated circuit successfully eliminated the previous static-1 timing hazard? Specify the time scale!

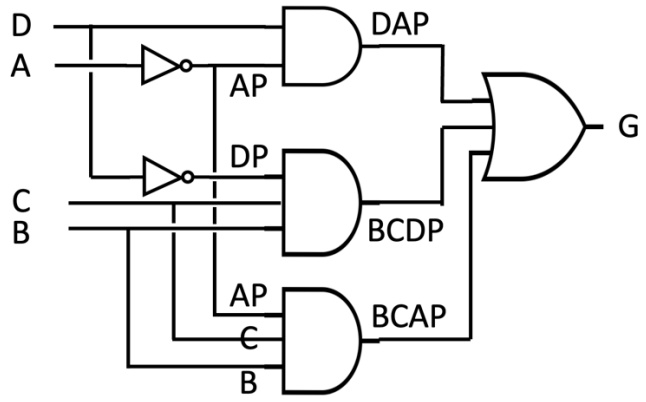

Fig. 2, circuit implementing of $G(A, B, C, D)$

Experiment 2: (*40 Points***)**

Let's implement the timing hazard free circuit $G(A, B, C, D)$, shown in Fig. 2 in the pre-lab, with Emona board. We would need four different gates to implement this circuit in Emona.

Device #	Module Name
1	Dual AND Module
2	Inverter
1	Triple OR Module
2	Triple AND Module

i. We have 4 input and 1 output in this circuit, however, we have only 4 channels to monitor both input/output signals at once. Besides the binary counter input source, we could use a "SWITCHES" module to help us manually control one of the inputs, for example A. Monitor the other three inputs via Channels A, B, and C, and the output via Channel D. Complete the truth table from your waveforms, take two screenshots, one when input A=0, one when input A=1, save them as JPG or PNG, and include in your report. Verify that it agrees with the minterm list defining the function $A(A, B, C, D)$.

A	B	C	D	$G(A, B, C, D)$
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	

0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Experiment 3: (*20 Points***)**

In this experiment you are given the logic diagram in Fig. 3. Make this circuit with Emona board with as fewer gates as possible, the fewer gates you used, the more points you would get. Note that we don't have NOR gate in Emona.

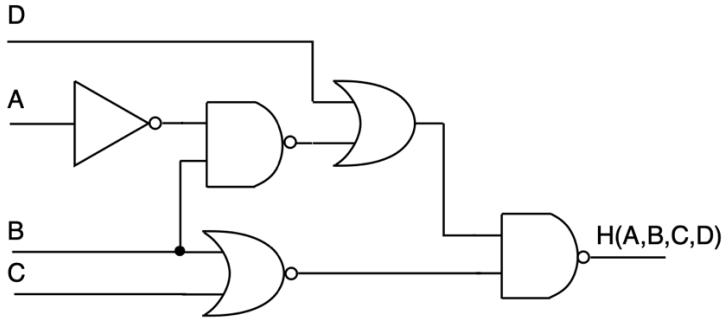

Fig. 3, given the logic diagram of function $H(A, B, C, D)$

i. Obtain the expression of function $H(A, B, C, D)$ and complete the truth table. Simplify it using Boolean algebra. Draw the equivalent simplified circuit. Make this circuit with Emona board. You may use "SWITCHES" module if necessary. Complete the truth table from your waveforms, take screenshot and include in your report. Verify that it agrees with the minterm list defining the function $H(A, B, C, D)$.

A	B	C	D	$H(A, B, C, D)$
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	

0 1 0 0	
0 1 0 1	
0 1 1 0	
0 1 1 1	
1 0 0 0	
1 0 0 1	
1 0 1 0	
1 0 1 1	
1 1 0 0	
1 1 0 1	
1 1 1 0	
1 1 1 1	