Kennesaw State University **EE2501 Lab 4: Implementation of Adders**

Name (PRINT): Last_____ First _____ **Date**:_____

Section(Circle): Tuesday/Thursday **Lab Partner Name** (PRINT): Last_____ First_____

*Approval by Instructor: Completed*_____ *Functional*_____ *Incompleted*_____

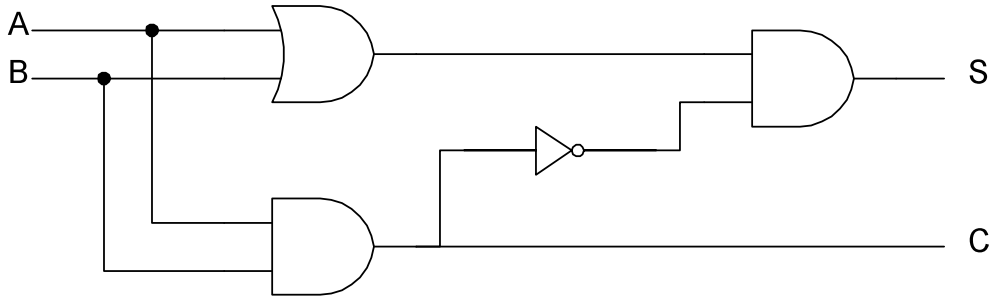
Objective:

To verify and apply techniques to build half adders and full adder to perform additions using gates.

For each part of the procedure, show the number of that section and include a logic diagram of the circuit, truth table for the circuit, and any other necessary information.

Adder Implementation

1. Construct a binary half-adder and record the truth table for this circuit.



2. Using the two half adder blocks you have built above and an OR gate, build a Full adder that has C_{in}. Provide complete schematic and record the truth table for this full adder.

3. If you want to build full adders to add two n-bit numbers with C_{in} and C_{out}, how can you build this module? Draw the block diagram of this full adder.

VHDL Lab

HDL is hardware description language to describe the structure and behavior of electronic circuits, and most commonly, digital logic circuit. We will practice writing VHDL codes to simulate the full adder implemented in the above procedure.

1. Go to https://www.edaplayground.com/ and create login/passwd.

2. Choose VHDL in the “Testbench+Design” on the left below the “Languages & Libraries”

3. Select "Aldec Rivera Pro 2014.06" under the "Tools and Simulators" combo box.

4. Choose “Open EPWave after run" in the check box. You can get the test results in a waveform-type display after you run the simulation by clicking RUN at the top of the display.

5. Click “VHDL” in “Examples” and choose “VHDL - Basic OR Gate” on the top.

Now, you see two files, one is testbench.vhd on your left window, and design.vhd on your right window with the title, Simple OR gate design.

6. Click “Run” and you should be able to see the generated waveform. Print this page and attach in your report.

7. Write your own full-adder in VHDL and submit the original code with printed waveform.